VERTICAL FIELD EFFECT TRANSISTORS INCLUDING CONFORMAL MONOCRYSTALLINE SILICON LAYER ON TRENCH SIDEWALL

Abstract of the Disclosure

Vertical field effect transistors are fabricated by depositing a vertical channel on a microelectronic substrate at a thickness along the microelectronic substrate that is independent of lithography, the vertical channel extending orthogonal to the microelectronic substrate. Source and drain regions are formed at respective opposite ends of the vertical channel, and an insulated gate is formed adjacent the vertical channel. More specifically, a first doping layer is formed on a microelectronic substrate, an intermediate layer is formed on the first doping layer opposite the substrate and a second doping layer is formed on the intermediate layer opposite the first doping layer. A trench is then formed in the first doping layer, the intermediate layer and the second doping layer, the trench including a trench sidewall. The trench sidewall is lined with a conformal amorphous silicon layer. The conformal silicon layer on the trench sidewall includes a first end portion adjacent the first doping layer, a second end portion adjacent the second doping layer, and a middle portion between the first and second end portions adjacent the intermediate layer. The amorphous silicon layer is then crystallized. The trench that is lined is plugged, for example with high dielectric constant material. Annealing is performed to dope the first end portion and the second end portion with dopants from the first and second doping layers respectively. The intermediate layer is removed adjacent the middle portion to expose at least some of the middle portion. A gate insulating layer is formed on the middle portion that is exposed, and a gate electrode is formed on the gate insulating layer, opposite the middle portion. One or more drain contacts may be formed in the microelectronic substrate prior to forming the first doping layer, for example using silicide. Moreover, one or more source contacts may be formed on the second end of the conformal silicon layer.